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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,365	01/11/2002	Xiaobao Wang	015114-054910US	8233

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EXAMINER
CHANG, DANIEL D

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,365	WANG ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Acknowledgement

Receipt is acknowledged of the Amendment filed June 27, 2003.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Asano et al. (US 4,719,369, "Asano" hereinafter).

Regarding claims 1 and 2, in figures 1 and 2, Asano teaches an integrated circuit comprising:

a first transistor (20 or 21) coupled to an off-chip resistor (22 or 23, col. 4, lines 7+);

an analog-to digital converter (30) coupled to the first transistor;

a digital encoder circuit (31) coupled to receive output signals of the analog-to-digital-converter; and

an impedance matching circuit (2-5, 7-10, 12-19) coupled to receive output signals of the digital encoder circuit, the digital encoder output signals characterized by values (col. 4, lines 8+), wherein the impedance matching circuit comprises a plurality of second transistors (2-5, 7-10) coupled in parallel, wherein an impedance of the impedance matching circuit increases (when more transistors 2-5, 7-10 are turned OFF) in response to a change in the values of the digital encoder output signals (26, 27) in a first direction and wherein the impedance of the

impedance matching circuit decreases (when more transistors 2-5, 7-10 are turned ON) in response to a change in the values of the digital encoder output signals (26, 27) in a second direction.

Regarding claim 3, in figures 1 and 2, Asano shows that the impedance matching circuit is coupled in parallel (2-5, 7-10) with an I/O pin (a common output node between transistors 5 and 10) of the integrated circuit.

Regarding claim 4, in figures 1 and 2, Asano shows that the impedance matching circuit is coupled in series (from VDD or GND to I/O pin) with an I/O pin (a common output node between transistors 5 and 10) of the integrated circuit.

Regarding claim 5, in figures 1 and 2, Asano shows that the impedance matching circuit is coupled to a buffer circuit (1, 6, 11) that is coupled to the I/O pin.

Regarding claim 6, in figures 1 and 2, Asano shows a plurality of impedance matching circuits (1st impedance matching circuit 2-5, 12-15; and 2nd impedance matching circuit 7-10, 16-19) coupled to receive output signals (26, 27) of the digital encoder circuit (a combination of 31 in 24 and 25), wherein the plurality of impedance matching circuits each comprises a plurality of transistors coupled in parallel (2-5 and 7-10).

Regarding claims 7 and 8, it is well known in the art that it is a common practice that a plurality of resistors and comparators are used in the analog-to-digital converter (see US 5,721,548), even if it is not, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Regarding claims 9 and 10, in figures 1 and 2, Asano shows that the plurality of second transistors of the impedance matching circuit comprises four (2-5) or five (1-5) transistors coupled in parallel.

Method claims 11-20 are essentially the same in scope as apparatus claims 1-10 and 21-28 and are rejected similarly.

Regarding claim 14, the plurality of second signals (26 or 27 comprises 4 bits) is fewer in number than the plurality of digital signals (output of A/D 30 comprises 5 bits. See col. 4, lines 8+).

Claims 21-28 are rejected similarly with claims 1-10. Regarding the limitation, "programmable logic circuitry" in claim 21, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Response to Arguments

Applicant's arguments filed June 27, 2003 have been fully considered but they are not deemed to be persuasive.

Applicant has amended claims 1, 14, and 21 to distinguish over Asano et al. (US 4,719,369). However, the cited reference, Asano et al. discloses all of the claimed features of these claims.

Applicant argues, on page 9 of the Amendment filed June 27, 2003, that Asano teaches that "the transistor gate width can only be trimmed in manner that causes a decrease in the

impedance of the output circuit." but "the claimed invention, on the other hand, can increase and decrease the impedance of the impedance matching circuit". However, the terms, "decrease" and "increase" are relative terms. Therefore, when more transistors 2-5, 7-10 are turned OFF in order to compensate for the variations in the output resistance (see col. 1, lines 58+; col. 3 lines 57 - col. 4, lines 56), the present impedance respect to the previous impedance of the impedance matching circuit increases because the output resistance will continuously vary due to the variations of the element or variations in power supply or temperature (col. 1, lines 58+); and when more transistors 2-5, 7-10 are turned ON in order to compensate for the variations in the output resistance, the present impedance respect to the previous impedance of the impedance matching circuit decreases. Therefore, rejection of claims 1-28 are maintained as stated above.

Conclusion

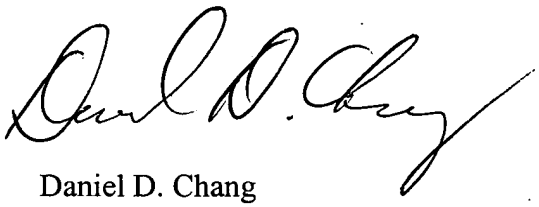
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Daniel D. Chang
Primary Examiner
Art Unit 2819

DC
July 16, 2003

DANIEL CHANG
PRIMARY EXAMINER